2123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/788,219
Filed: February 16, 2001
Inventor(s):
Jeffrey L. Kodosky, Hugo Andrade,
Brian Keith Odom and Cary Paul Butler

Title: System and Method for Converting a Graphical Program Including a Structure Node into a Hardware Implementation

Examiner: Frejd, Russell Warren
Group/Art Unit: 2123
Atty. Dkt. No: 5150-23006

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313-1450 on the date indicated below.

Jeffrey C. Hood
Name of Registered Representative

Signature 5/22/2003 Date

RESPONSE TO OFFICE ACTION OF MARCH 25, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of March 25, 2003, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE CLAIMS:

Please amend claim 23 as follows:

23. (Amended) The system of claim 22, wherein the structure node is one of an iteration node or a looping node;

wherein the structure node includes at least one of a period parameter and a phase delay parameter, wherein the period parameter indicates a period of execution for cycles of the structure node, and wherein the phase delay parameter indicates a phase delay of cycles of the structure node.